REMARKS

The present Amendment corrects some minor typographical errors in the specification; inserts the serial number of an application previously identified only by attorney docket number; amends Claims 6, 11, 24, and 30; cancels claim 12; and adds new Claims 32-95. Upon entry of this amendment, claims 1, 3, 4, 6, 8-11, 13-17, and 24-95 will be pending. Also enclosed are new formal drawings, as called for in the Notice of Allowability issued 2 July 2001. This Amendment is being submitted with a Request for Continued Examination (RCE) and an Information Disclosure Statement submitting additional references for the Examiner's consideration.

The present RCE is being filed after issuance of a Notice of Allowability to add claims drawn to additional subject matter disclosed in the specification but not previously claimed and to afford the Examiner an opportunity to consider additional references not previously of record. The undersigned looks forward to meeting with Examiner Collins to discuss this application at noon on Tuesday, 9 October.

Applicants believe that upon entry of this Amendment all of the Claims in the application will be in condition for allowance, prompt notice of which is courteously solicited. If the Examiner has any questions or would like to discuss any aspect of this case, the undersigned would welcome a telephone call at the number listed below.

Respectfully submitted,

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Enclosures:
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Appendix (Marked-up version of Claims)

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APPENDIX – SPECIFICATION MARKED TO SHOW CHANGES

The paragraph appearing at page 12, lines 15-22 has been amended as follows:

> The semiconductor wafer with the seed layer 425 is subject to a subsequent electrochemical copper deposition process. The electrochemical copper deposition process is executed so as to form numerous nucleation sites for the copper deposition to thereby form grain sizes that are substantially smaller than the characteristic dimensions of the via 420 and trench 415. An exemplary structure having such characteristics is illustrated in Fig. 2E ~~4E~~ wherein layer 440 is a layer of copper metallization that has been deposited using an electrochemical deposition process.

The paragraph extending from page 13, line 12, to page 14, line 4 has been amended as follows:

> A comparison between Figs. 2E and 2F~~4E and 4F~~ reveals that an increase in the grain size of the copper layer 440 has taken place. Traditionally, the change in the grain size has been forced through an annealing process. In such an annealing process, the wafer is subject to an elevated temperature that is substantially above the ambient temperature conditions normally found in a clean room. For example, such annealing usually takes place in a furnace having a temperature generally around or slightly below 400 degrees Celsius, or about half of the melting temperature of the electrodeposited copper. Annealing steps are normally performed at a temperature of at least 25 percent of the melting point temperature of the material as measured on an absolute temperature scale. As such, a separate annealing step is performed on the wafer using a separate piece of capital equipment. Such an annealing step is usually performed for each layer of metallization that is deposited on the wafer. These additional steps increase the cost of manufacturing devices from the wafer and, further,

provide yet another step in which the wafer may be mishandled, contaminated or otherwise damaged.

The paragraph appearing at page 15, lines 5-14 has been amended as follows:

The electrochemical plating solution may be Enthone-OMI Cu Bath M Make-up Solution having 67 g/l of $CuSO_4$~~CuSO4~~, 170 g/l of H_2SO_4~~H2SO4~~, and 70 ppm of HCl. The additive solutions utilized may be Enthone-OMI Cu Bath M-D (6.4 ml/l - make-up) and Enthone-OMI Cu Bath M LO 70/30 Special (1.6 ml/l - make-up). The flow rate through the cup 25 of this solution may be approximately 1.0 - 10 GPM (preferably 5.5 GPM) and the plating temperature may be between about 10-40 degrees Celsius (preferably 25 degrees Celsius). The plating bath could alternatively contain any of a number of additives from manufacturers such as Shipley (Electroposit 1100), Lea Ronal (Copper Gleam PPR), or polyethylene glycol (PEG). An alkaline plating bath suitable for electroplating microelectronic components is set forth in co-pending provisional patent application U.S.S.N. 60/085,675, filed 15 May 1998 and entitled "PROCESS AND PLATING SOLUTION FOR ELECTROPLATING A COPPER METALLIZATION LAYER ONTO A WORKPIECE" ~~(Attorney Docket No. SEM4492PO250US; Corporate Docket No. P98-0039)~~ which is hereby incorporated by reference.

APPENDIX – CLAIMS MARKED TO SHOW CHANGES

6. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

depositing copper into the recessed microstructures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece and the deposited copper to an elevated temperature annealing process at a temperature at or below about 250 degrees Celsius for a time period of no longer than 15 minutes, which time period ~~that~~ is sufficient to increase the grain size of the deposited copper.

11. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed microstructures with a metal seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

annealing the electrochemically deposited copper for a predetermined period of time at an elevated temperature selected to be below a predetermined temperature at which ~~time~~ the low-K dielectric layer would substantially degrade ~~for a predetermined period of time~~; and

APPENDIX – CLAIMS MARKED TO SHOW CHANGES

6. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

depositing copper into the recessed microstructures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece and the deposited copper to an elevated temperature annealing process at a temperature at or below about 250 degrees Celsius for a time period of no longer than 15 minutes, which time period ~~that~~ is sufficient to increase the grain size of the deposited copper.

11. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed microstructures with a metal seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

annealing the electrochemically deposited copper for a predetermined period of time at an elevated temperature selected to be below a predetermined temperature at which ~~time~~ the low-K dielectric layer would substantially degrade ~~for a predetermined period of time~~; and

removing copper metallization from the surface of the workpiece except from the recessed microstructures, after annealing of the copper.

24. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a seed layer for subsequent ~~electrochemical~~ electrolytic copper deposition;

~~electrochemically~~ electrolytically depositing a copper layer onto the surface of the workpiece using an electrolytic process generating copper grains that are sufficiently small to substantially fill the recessed microstructures; and

subjecting the ~~electrochemically~~ electrolytically deposited copper layer to an annealing process at a temperature at or below about 250 to 300 degrees Celsius to increase the copper grain size.

30. (Twice Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at lest one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a barrier layer for subsequent ~~electrochemical~~ electrolytic copper deposition;

~~electrochemically~~ electrolytically depositing a copper layer to the surface of the workpiece using an electrolytic process that generates copper grains having a size sufficiently small to substantially fill the recessed microstructures; and

subjecting the ~~electrochemically~~ electrolytically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.